Amendments to the Claims

The following listing of claims will replace all prior versions and listings of the claims in the application:

Listing of Claims:

1. (Original) A method of testing memory, comprising:

executing each instruction of a plurality of test instructions in sequence, each said instruction having an inactive repeat control field except for a last instruction of each of one or more groups of one or more instructions to be repeated, each said last instruction having an active repeat control field;

for each instruction having an active repeat control field:

executing in sequence the instructions of the group of instructions with which said each instruction is associated for a predetermined number of repeat cycles for said group; and

for each said repeat cycle, modifying predetermined fields of each instruction in accordance with a predetermined field modification instructions for each said repeat cycle.

2. (Original) A method as defined in claim **1**, further including, prior to said executing each instruction:

loading into a first repeat instruction address register, the address of the first instruction in the group of instructions;

loading into a repeat cycle register a value indicating the number of repeat cycles to be performed for the group; and

loading field modification commands for each repeat cycle into a field modification register associated with said each repeat cycle.

3. (Original) A method as defined in claim **1**, said modifying predetermined fields including modifying the instruction field to a complementary value.

4. **(Original)** A method as defined in claim **3**, said modifying predetermined fields including modifying the least significant bit of the instruction field to a complementary value.

5. **(Original)** A method as defined in claim **1**, said modifying predetermined fields including, when a first group of instructions is nested within a second group of instructions, generating modified field modification instructions from the field modification instructions associated with said first and second groups.

6. **(Original)** A method as defined in claim **5**, said generating modified field modification instructions including comparing corresponding modification instructions associated with each said repeat cycles and generating a no change instruction when corresponding instructions are the same and generating a change instruction when corresponding instructions are different.

7. (Original) A method of testing memory, comprising:

loading a sequence of instructions into a sequence of instruction registers, each instruction having an inactive repeat control field except for the last instruction of each group of one or more instructions to be repeated;

loading into a first repeat instruction address register the address of the first instruction in the group of instructions;

loading into a register a value indicating a number of repeat cycles to be performed;

for each said repeat cycles, loading field modification commands into an associated field modification register;

executing each instruction of said sequence of instructions in sequence;

for each instruction having an active repeat command:

executing in sequence each instruction between and including the instruction located at the address stored in said address register and the instruction containing the said active repeat command for each of a number of repeat cycles specified in said repeat cycle register;

for each repeat cycle, modifying predetermined fields of each instruction in accordance with field modification instructions stored in said associated cycle modification register.

8. (Original) A method as defined in claim **7**, each said instructions having a next instructions field containing a one or more conditions fields for determining the next instruction to be executed.

9. (Original) A method as defined in claim **8**, said next conditions field including a repeat loop done condition, said repeat loop done condition being active when said repeat control field is active and being inactive when said repeat control field is inactive.

10. (Original) A method as defined in claim **8**, each said instructions further including address sequencing fields, an operation select field, an Inhibit Data Compare field, and an Inhibit Last Address Count field.

11. (Original) A method as defined in claim **10**, said field modification instructions including a sequence of binary bits for modifying said address sequencing fields, operation select field, inhibit data compare and inhibit last address count fields.

12. (Original) In an memory test controller for testing a memory array, said controller having a test instruction register array having registers for storing a plurality of test instructions, each register having instruction fields for storing memory addressing sequencing data, write data sequencing data, expect data sequencing data and operation data specifying an operation to be performed on said memory array, the improvement comprising:

a repeat module for repeating a group of one or more test instructions with modified data, said repeat module including storage means for storing instruction field modification data; and each register of said test instruction register array including an instruction field for enabling or disabling said repeat module.

13. (Original) In a memory test controller as defined in claim **12**, said repeat module including first and second repeat loop circuits, each repeat loop circuit being operable for repeating a group of one or more instructions with modified data for each of a predetermined number of repeat cycles, each said repeat loop circuit including a plurality of storage registers for storing instruction modification data associated with each said repeat cycle.

14. (Original) In a memory test controller as defined in claim **13**, each said repeat loop circuit including means for selecting said storage registers in predetermined sequence and outputting the contents thereof as repeat loop output data.

15. (Original) In a memory test controller as defined in claim **14**, said means for selecting including a counter having a counter output and responsive to said an enable input, and a multiplexer having a select input for receiving said counter output and having inputs connected to each said storage registers and a null input.

16. (Original) In a memory test controller as defined in claim **13**, said repeat module further including:

means for combining the outputs of said repeat loop circuits to produce a repeat module output; and means for combining said repeat module output with corresponding current data to produce new instruction data for execution of said operation.

17. (Original) In an embedded memory test controller for an integrated circuit having embedded memory, the improvement comprising:

first and second repeat loop circuits for use in repeating a respective group of test instructions, each repeat loop circuit having:

a plurality of repeat registers for storing instruction field modification data for use in modifying said instructions of said respective group; and

means for selecting each said repeat registers in predetermined sequence and outputting the contents thereof as selected modification data;

means for enabling one or both of said first and second repeat loop circuits;

means for combining the selected modification data output from said first and second repeat loop circuits with the repeat loop data output by the second repeat loop circuit to produce modified modification data; and

means for modifying the contents of instruction fields of an instruction with the modified modification data output by said means for combining.

18. (Original) A memory test controller as defined in claim **17**, said means for selecting including:

a counter for producing a register select output up to a predetermined repeat cycle count; and

a selector having a select input for receiving said register select output and outputting the contents of a selected repeat register.

19. (Original) A memory test controller as defined in claim **18**, said means for enabling including a command decoder responsive to a repeat command for producing a repeat loop enabling signal for each said repeat loop circuits;

means responsive to said enabling command and an active operation complete signal for causing each said counter to increment its count; and

means for resetting each said counter when its count reaches said predetermined repeat cycle count.

20. (Original) A memory test controller as defined in claim **19**, said means for combining the contents of a selected register being exclusive-OR gate means.

21. (Original) A memory test controller as defined in claim **17**, further including means for asserting a repeat loop done signal when both of said repeat loop circuits have completed execution.

22. (Original) In an embedded memory test controller for an integrated circuit having embedded memory, the improvement comprising:

an instruction repeat module having:

first and second repeat loop circuits, each repeat loop circuit having:

a plurality of repeat registers for storing instruction modification data associated with a repeat cycle;

means for selecting one of said repeat registers and outputting selected instruction modification data including:

means for storing the number of repeat cycles to be performed;

a counter for incrementally producing a register select output up to a value stored in said means for storing; and

a selector connected to each said repeat registers and having a select input for receiving said register select output and outputting the contents of a selected repeat register;

means responsive to a repeat control field of a current instruction for enabling one or both of said first and second repeat loop circuits including:

a command decoder responsive to said repeat control field for producing a repeat loop enabling signal for each said repeat loop circuits; and

means responsive to said enabling command and an active operation complete signal for causing said counter in an active repeat loop circuit to increment its count; and

means for disabling each said counter when its respective count reaches the value of stored in its respective means for storing;

exclusive-OR gate means for modifying selected instruction modification data from each said repeat loop circuit to produce modified instruction modification data;

means for generating a repeat loop done signal when both of said repeat loop circuits have completed execution; and

means for modifying instruction fields of a current instruction with the modified instruction modification data output by said means for modifying.

23. (Original) In a test controller as defined in claim **22**, each said repeat registers being a 5-bit register including one bit associated with five address sequencing command fields, one bit associated with a WriteData command field, one bit associated with an InhibitDataCompare command field and one bit associated with an InhibitLastAddressCount command field.

24. (Original) A test controller for use in testing memory imbedded in an integrated circuit, comprising:

a scannable microcode register array having one or more instruction registers for storing a plurality of test instructions for performing a test of said memory in accordance with a predetermined test algorithm;

a pointer controller for selecting one of said test instructions for execution and determining a next instruction for execution in accordance with conditions stored in each said test instruction;

an instruction repeat module for reading address sequencing, write data sequencing, expect data sequencing data from a current test instruction and outputting address sequencing, write data sequencing, expect data sequencing data, said repeat module being responsive to instruction repeat data in said current test instruction for repeating an operation specified in said test instruction with different data;

a sequencer responsive to an operation code in said current instruction for performing a predetermined operation on said memory under test; and

an address generator and a data generator responsive to said output address sequencing, write data sequencing, expect data sequencing data for application to a memory under test in accordance with an operation specified in said current instruction.

25. (Original) A test controller as defined in claim **24**, said repeat module including:

at least one repeat loop circuit responsive to an instruction repeat control field for providing instruction modification commands for each of one or more instruction repeat cycles and including:

first storage means for storing instruction field modification commands;

second storage means for storing a number of repeat cycles to perform in a repeat operation;

circuit means responsive to a pointer controller control signal and a sequencer control signal for enabling said repeat loop circuit;

circuit means for signaling the end of an instruction repeat operation to said pointer controller;

circuit means for providing an instruction address of the first instruction of a sequence of one or more instructions to be repeated; and

circuit means for modifying instruction fields in accordance with said instruction field modification commands and outputting instructions to said address generator and a data generator.

26. (Original) A test controller as defined in claim **25**, said module comprising two of said repeat loop circuits, each said repeat loop circuits having respective first and second storage means.

27. (Original) A test controller as defined in claim **26**, said first storage means including a plurality of storage registers for storing a plurality of single-bit instruction modification commands, each said commands being associated with one or more instruction fields and each said storage registers being associated with one repeat cycle.

28. (Original) A test controller as defined in claim **27**, each said repeat loop circuit further including means for selecting one of said storage registers for each repeat cycle, said means for selecting including a counter having a counter output and responsive to an enable input, and a multiplexer having a select input for receiving said counter output and having inputs connected to each said storage registers and a null input.